Optimizing Gate Driver to Smooth Gate Waveform

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Abstract

When using IGBT for power system design, smooth gate waveform is expected by engineers. Spikes, oscillations on the switching edges are the troubles. It makes the system unstable, unreliable and low efficiency. This paper discusses what kind reasons cause the spike and oscillation during IGBT switching, and, how to optimizing the gate driver to resolve it.

1. Spike and oscillation on the gate waveforms

1.1. Spike on the rising edge

When driving an IGBT turn on, sometimes, spike occurs on the gate waveform (Fig.1).

Fig.1  Spike on gate waveform

As we known, while the $V_{GE}$ passes the $V_{GE(th)}$, IGBT begins to conduct, then $I_C$ increases and $V_{CE}$ decreases. Meanwhile, the $dV_{CE}/dt$ causes current ($I_{GC}$) to flow through the $C_{GC}$. This current, along with $I_G$, charge the $C_{GE}$ together(Fig.2). If the value of $dV_{CE}/dt$ is high, $I_{GC}$ surges into $C_{GE}$ and pushes the $V_{GE}$ to peak rapidly.
When $V_{CE}$ decreases lower than $V_{GE}$, $I_{GC}$ will be reversed. During this time, $I_{GC}$ share the charge current $I_G$ then $V_{GE}$ falls back to miller plateau. Similar with the previously situation, the high $dV_{CE}/dt$ pulls $V_{GE}$ to sink rapidly.

1.2. Oscillation on the Miller plateau

In another case, oscillation can be found on miller plateau (Fig.3). This condition can make gate risk and causes high switching losses.

![Fig.3 Oscillation on the gate waveform](image-url)
As the equivalent model, the gate drive output circuit is illustrated a series RLC circuit. RLC correspond to \( R_G, L_G, L_S \) and \( C_{GE} \) respectively (Fig.4).

Fig.4 Equivalent circuit of Gate driver

Generally, we think there’re several reasons may cause gate drive oscillation. First, a badly circuit board trace layout causes. Once the inductance of \( L_G \) is large enough to make the current phase shifted, oscillation can be established. Second, lower resistance of RLC circuit is easier to oscillate. When \( R_G \) is configured with a low value resistor, larger \( I_G \) makes RLC oscillator can be excited easier. Third, high \( dV_{CE}/dt \) makes \( I_{GC} \) increasing then enhances the possibility of excitation. However, noise is the mainly element that high \( dV_{CE}/dt \) induces.

1.3. \( I_{GC} \) charges low-side IGBT

Generally, high-side IGBT is turning on while low-side IGBT is in off state, a rapidly \( dV_{CE}/dt \) which is induced by high-side IGBT switching operation causes the \( I_{GC} \) to charge the low-side IGBT gate, then, it raises \( V_{GE} \) up (fig.5).

Fig.5 Miller current flow when IGBT in off stat
When the amplitude of $V_{GE}$ exceeds the $V_{GE(th)}$, IGBT starts to turn on. If the gate driver cannot sink the current, the risk of half bridge shoot-through will increase.

2. Optimizing Gate Driver

2.1. Configure $R_G$ with suitable value

In usually, only single gate resistor $R_G$ is used to adjust charging and discharging current $I_G$, just like Fig. 2 has shown. This, to avoid high $dV_{CE}/dt$ can trigger IGBT turn on; the minimum value of $R_G$ is determined by the equation as below (EQU1):

$$dV_{CE}/dt = (V_{GE(th)} + V_{ce(sat).L}) / \left[ (R_{G.int} + R_G) * C_{CG} \right] \tag{EQU.1}$$

Where the $V_{ce(sat).L}$ is the saturation voltage of PNP transistor.

Sometimes, in order to control the rise time and fall time individually, two gate resistors called $R_{G(on)}$ and $R_{G(off)}$ are utilized (Fig.6).

![Fig.6 R_{G(on)} and R_{G(off)} separated](image)

Then, the value of $R_{G(on)}$ and $R_{G(off)}$ are determined by the equations respectively as below (Equ.2 & Equ.3)

$$\text{Turn on: } dV_{CE}/dt = V_{GE(th)} + V_{ce(sat).H} / \left[ (R_{G.int} + R_{G(on)}) * C_{CG} \right] \tag{EQU.2}$$

$$\text{Turn off: } dV_{CE}/dt = V_{GE(th)} + V_{ce(sat).L} / \left[ (R_{G.int} + R_{G(off)}) * C_{CG} \right] \tag{EQU.3}$$

Where the $V_{ce(sat).H}$ is the saturation voltage of NPN transistor.

2.2. Make lower impedance power supply

IGBT gate driver needs low impedance power supply to provide highly responsible dynamic current. In idealization, when analyzing the gate drive circuit loop, the impedance of positive and negative power supplies are assumed to be zero. In realized design, ceramic capacitors with high frequency and low impedance characteristics are used. To provide very low impedance and very good high
frequency response, the bypass capacitors should be placed as close as possible to totem-pole transistors (Fig.7).

![Fig.7 Bypass capacitors layout](image1)

The layout must minimize the parasitic inductance between the output of driver and gate resistor. Therefore, it’s helpful to keeping the loop area as small as possible in both charging and discharging current loop.

**2.3. External gate-emitter capacitor C_G**

In common application, an external gate-emitter capacitor is located near the gate terminal (Fig.8).

![Fig.8 Gate terminal bypass capacitor C_g](image2)

Generally, it's used to bypass the I_GC. Since this capacitor is located between the gate terminal and emitter terminal, not only the I_GC but also the I_G is shared by C_g. And therefore, when I_G is shared, the current which is charging or discharging Q_G will be decreased. So that, the ramp of rising edge and falling edge will be slow down, and, the dV_{CE}/dt will decrease.
2.4. Experiments

The following waveforms are showing, what kind of changes on the gate waveform when the $R_G$ or $C_G$ is configured with various value.

<table>
<thead>
<tr>
<th>$R_G = 20 \ \Omega$, $C_G = 1 \ \text{nF}$</th>
<th>$R_G = 36 \ \Omega$, $C_G = 1 \ \text{nF}$</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Waveform 1" /></td>
<td><img src="image2.png" alt="Waveform 2" /></td>
</tr>
<tr>
<td>$R_G = 36 \ \Omega$, $C_G = \text{NA}$</td>
<td>$R_G = 36 \ \Omega$, $C_G = 3.3 \ \text{nF}$</td>
</tr>
<tr>
<td><img src="image3.png" alt="Waveform 3" /></td>
<td><img src="image4.png" alt="Waveform 4" /></td>
</tr>
</tbody>
</table>

Fig.9 Gate waveforms with different $R_G$ and $C_G$ configuration

It’s obviously that, the procedure of optimization is effectively. The gate waveform becomes better step by step.

3. Conclusion

To smooth the gate waveform, all elements of gate driver and IGBT should be noticed. This paper discusses $R_G$ and bypass capacitors only. The other elements do not discussed, such as stray inductance of connect wire, $R_{GE}$, etc.

Reference